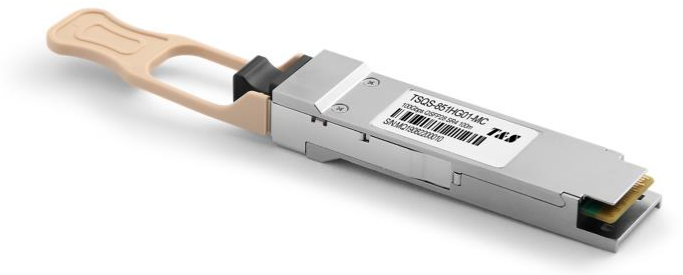
TSQS-851HG01-MC Optical Transceiver

Multi-mode 100G SR4 Transceiver, With Diagnostic Monitoring
4 channels full-duplex 100m Transceiver

Features

- Transmission data rate up to 25Gbps per channel
- 4 channels 850nm VCSEL array
- 4 channels PIN photo detector array
- Hot-pluggable QSFP28 form factor
- Low power consumption < 3.5W
- Single 1X12 MPO connector receptacle
  Hot-pluggable electrical interface
- Operating case temperature: 0°C~+70°C
- RoHS6 compliant (lead free)



Applications

- IEEE 802.3bm 100GBASE SR4
- Infiniband FDR/EDR

Description

The TSQS-851HG01-MC module is a highly integrated 4x25G transceiver focused on reach, bandwidth, density and cost for high port-count 100G systems, and client-side 100G interfaces. Each lane can operate at 25Gbps up to 70m using OM3 fiber or 100m using OM4 fiber. These modules are designed to operate over multimode fiber systems using a nominal wavelength of 850nm. The electrical interface uses a 38-contact edge type connector. The optical interface uses a 12-fiber MTP/MPO connector.

Absolute Maximum Ratings

These values represent the damage threshold of the module. Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions.

Parameters	Symbol	Min.	Max.	Unit
Power Supply Voltage	VCC	-0.5	+3.6	V
Storage Temperature	Tc	-40	+85	°C
Relative Humidity	RH	0	85	%

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Recommended Operating Environment

Parameter	Symbol	Min	Typical	Max	Unit
Power Supply Voltage	VCC	3.15	3.30	3.45	V
Supply current	Icc	-	-	1014	mA
Operating Case Temperature	Tca	0	-	70	°C

Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit
Transmitter					
Input differential impedance	Rin	-	100	-	Ω
Differential Input Voltage swing, per lane	Vin	300	-	1100	mV
Input Logic Level High	VIH	2.0	-	VCC+0.3	V
Input Logic Level Low	VIL	Vee	-	Vee+0.8	V
Receiver					
Output differential impedance	Rout	-	100	-	Ω
Differential Output Swing, per lane	Vout	500	-	800	mV
Output Logic Level High	VOH	2.0	-	VCC+0.3	V
Output Logic Level Low	VOL	0	-	+0.4	V

Transmitter Specifications – Optical

Parameter	Symbol	Min	Typical	Max	Unit
Signaling Speed per Lane[1]	-	25.78125 ± 100ppm			Gb/s
Center Wavelength	λ	840	850	860	nm
RMS spectral width	Δλ	-	-	0.6	nm
Average Launch Power per Lane	Po	-6	-	2.4	dBm
Transmit OMA per Lane	OMA	-6.4	-	3	dBm
Launch Power [OMA] minus TDEC per Lane	P-TDEC	-7.3	-	-	dBm
Extinction Ratio	ER	3	-	-	dB
Optical Return Loss Tolerance	ORL	-	-	12	dB
Encircled Flux	FLX	> 86% at 19 um < 30% at 4.5 um			dBm
Average launch power of OFF transmitter,	-	-	-	-30	dBm

each lane					
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}[2]	{ 0.3, 0.38, 0.45, 0.35, 0.41, 0.5}				

Receiver Specifications – Optical

Parameter	Symbol	Min	Typical	Max	Unit
Bit Rate per Channel[3]	DR	25.78125 ± 100ppm			Gb/s
Center Wavelength	λ	840	850	860	nm
Damage Threshold	DT	3.4	-	-	dBm
Average receive power, each lane[4]	RXPOW	-10.3	-	2.4	dbm
Unstressed Sensitivity (OMA) at 10 x 10-12 BER	RxOMA	-	-	3	dBm
Stressed Receiver Sensitivity (OMA) per Lane	SRS	-	-	-5.2	dBm
Vertical eye closure penalty, each lane	VECP	-	-	1.9	dB
Stressed eye J2 jitter, per Lane	J2	-	-	0.39	UI
Stressed eye J4 jitter, per Lane	J4	-	-	0.53	UI
OMA of each aggressor lane	-	-	3	-	dBm

Notes:
[1]. Transmitter consists of 4 lasers operating at a maximum speed of 25.78125Gb/s ±100ppm each.
[2]. Hit Ratio 1.5 x 10^{-3} hits/sample.
[3]. Receiver consists of 4 photodetectors operating at a maximum speed of 25.78125Gb/s ±100ppm each lane.
[4]. Minimum value is informative only and not the principal indicator of signal strength.

General Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Bit Rate (all wavelengths combined)[1]	BR	-	-	103.1	Gb/s
Bit Error Ratio (pre-FEC)[2]	BER	-	-	5x10^{-5}	-
Maximum Supported Distances					
Fiber Type	-	-	-	-	-
OM3 MMF[3]	LMAX1	-	-	70	m
OM4 MMF[3]	LMAX2	-	-	100	m

Notes:
[1] Supports 100GBASE-SR4 per IEEE 802.3bm.
[2] Tested with a 231 – 1 PRBS.
[3] Requires FEC on the host to support maximum distance, per 100GBASE-SR4.

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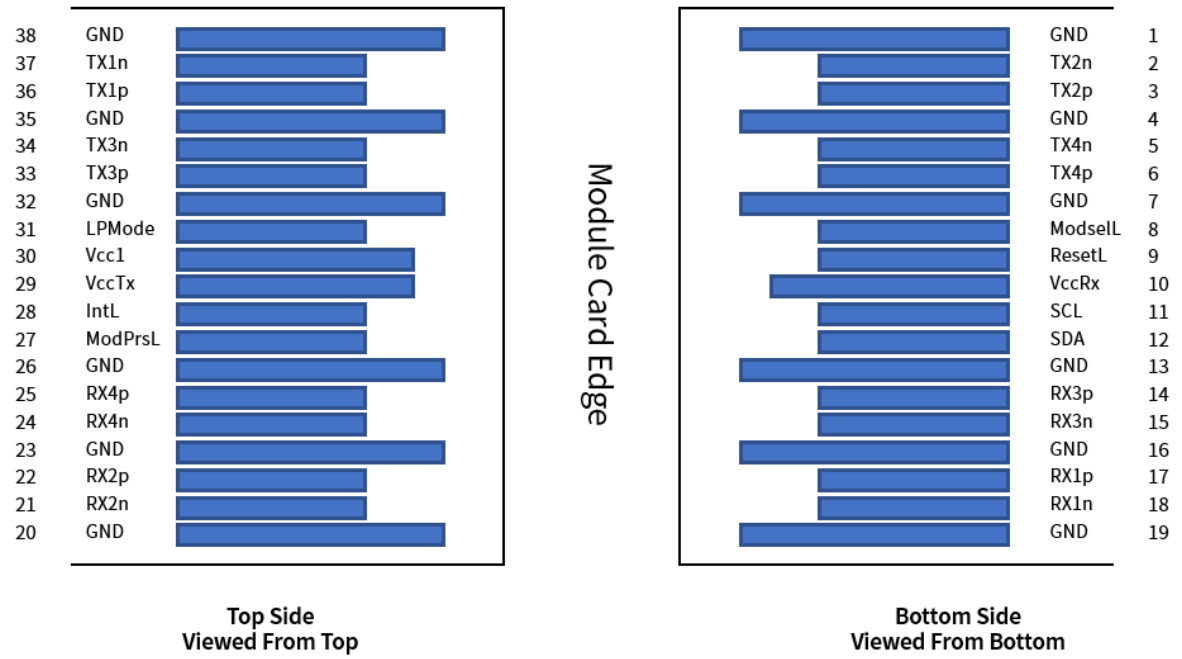
Qsfp Transceiver Electrical Pad Layout



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin Definition

Pin	Symbol	Name/Description
1	GND	Ground
2	Tx2n	Transmitter Inverted Data Input
3	Tx2p	Transmitter Non-Inverted Data Input
4	GND	Ground
5	Tx4n	Transmitter Inverted Data Input
6	Tx4p	Transmitter Non-Inverted Data Input
7	GND	Ground
8	ModSelL	Module Select
9	ResetL	Module Reset
10	VCC Rx	+3.3 V Power supply receiver
11	SCL	2-wire serial interface clock
12	SDA	2-wire serial interface data
13	GND	Ground
14	Rx3p	Receiver Non-Inverted Data Output
15	Rx3n	Receiver Inverted Data Output
16	GND	Ground
17	Rx1p	Receiver Non-Inverted Data Output

18	Rx1n	Receiver Inverted Data Output
19	GND	Ground
20	GND	Ground
21	Rx2n	Receiver Inverted Data Output
22	Rx2p	Receiver Non-Inverted Data Output
23	GND	Ground
24	Rx4n	Receiver Inverted Data Output
25	Rx4p	Receiver Non-Inverted Data Output
26	GND	Ground
27	ModPrsL	Module Present
28	IntL	Interrupt
29	VCC Tx	+3.3 V Power supply transmitter
30	VCC 1	+3.3 V Power Supply
31	LPMode	Low Power Mode
32	GND	Ground
33	Tx3p	Transmitter Non-Inverted Data Input
34	Tx3n	Transmitter Inverted Data Input
35	GND	Ground
36	Tx1p	Transmitter Non-Inverted Data Input
37	Tx1n	Transmitter Inverted Data Input
38	GND	Ground

Ordering Information

Part Number	Product Description
TSQS-851HG01-MC	QSFP28 100G SR4 100m@OM4 0°C ~ +70°C

References

1. SFF-8636 Specification for QSFP28.
2. Ethernet 100GBASE-SR4 IEEE802.3bm
3. 128GFC Specification, per ANSI T.11 FC-PI-6P.
4. IEEE 802.3bm, PMD Type 100GBASE-SR4 and CAUI-4.

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